N-Channel and P-Channel 20 V (D-S) MOSFET

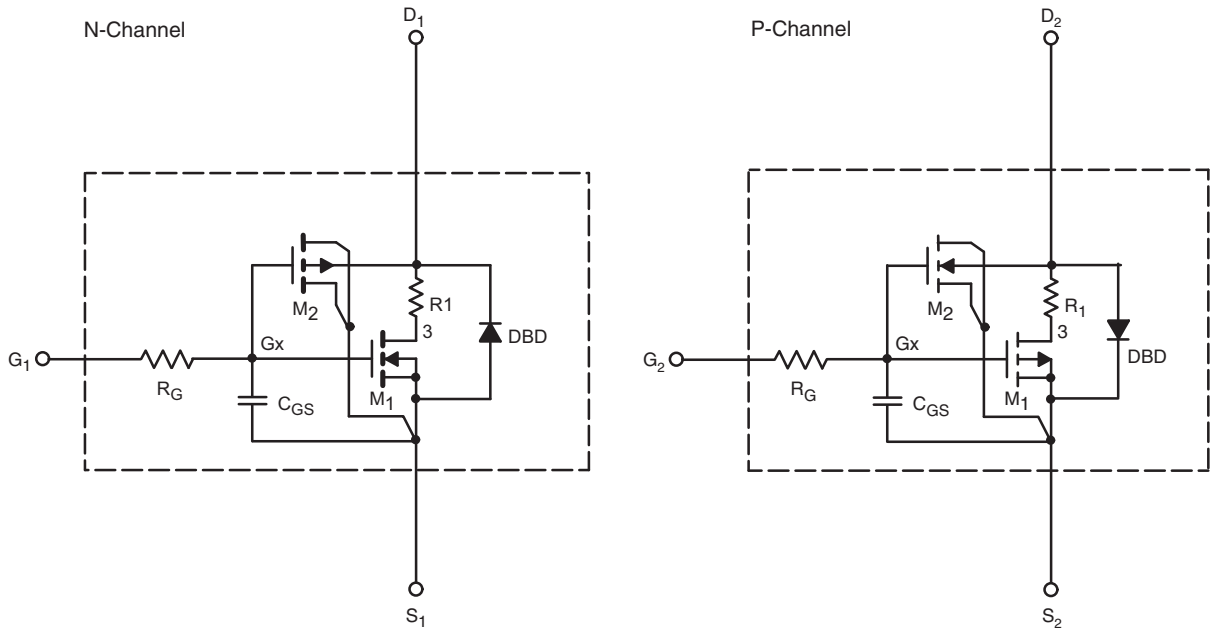
DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to + 125 °C temperature ranges under the pulsed 0 V to 4.5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage. A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

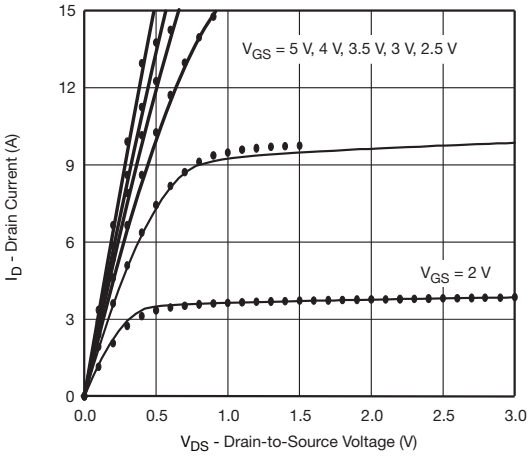
SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1.1	-	V
		V_{DS} = V_{GS}, I_D = - 250 µA	P-Ch	0.82	-	
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.2 A	N-Ch	0.033	0.032	Ω
		V_{GS} = - 4.5 V, I_D = - 2.9 A	P-Ch	0.080	0.074	
		V_{GS} = 2.5 V, I_D = 3.3 A	N-Ch	0.056	0.053	
		V_{GS} = - 2.5 V, I_D = - 2.3 A	P-Ch	0.11	0.113	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 4.2 A	N-Ch	11	12	S
		V_{DS} = - 10 V, I_D = - 2.9 A	P-Ch	7.7	7	
Diode Forward Voltage[a]	V_{SD}	I_S = 4.4 A	N-Ch	0.86	0.80	V
		I_S = - 3 A	P-Ch	0.84	- 0.80	
Dynamic[b]						
Input Capacitance	C_{iss}	N-Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz	N-Ch	346	350	pF
			P-Ch	335	340	
Output Capacitance	C_{oss}		N-Ch	82	82	
			P-Ch	104	105	
Reverse Transfer Capacitance	C_{rss}		N-Ch	48	50	
			P-Ch	93	95	
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 10 V, I_D = 5.5 A	N-Ch	6.1	7.7	nC
		V_{DS} = - 10 V, V_{GS} = - 10 V, I_D = - 3.7 A	P-Ch	11	10.5	
Gate-Source Charge	Q_{gs}	N-Channel V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 5.5 A P-Channel V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 3.7 A	N-Ch	3.1	3.7	
			P-Ch	4.6	5.3	
			N-Ch	0.85	0.85	
			P-Ch	0.75	0.75	
Gate-Drain Charge	Q_{gd}		N-Ch	0.95	0.95	
			P-Ch	2	2	

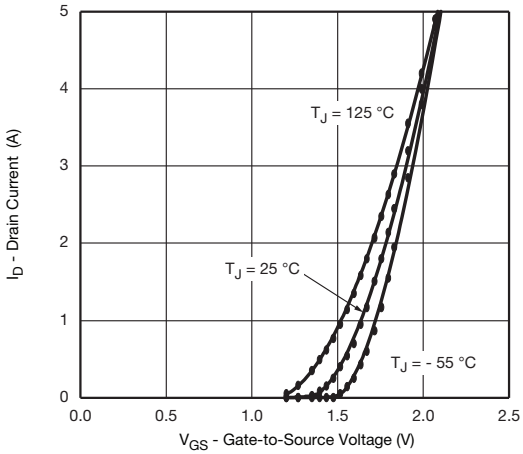
Notes

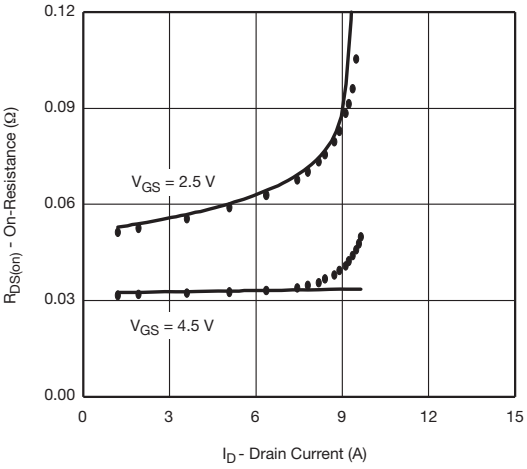
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

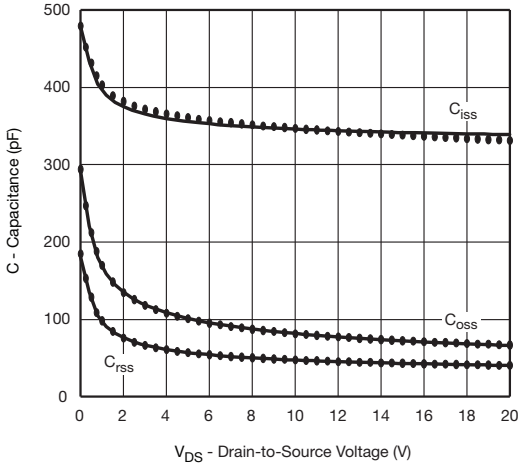
b. Guaranteed by design, not subject to production testing.

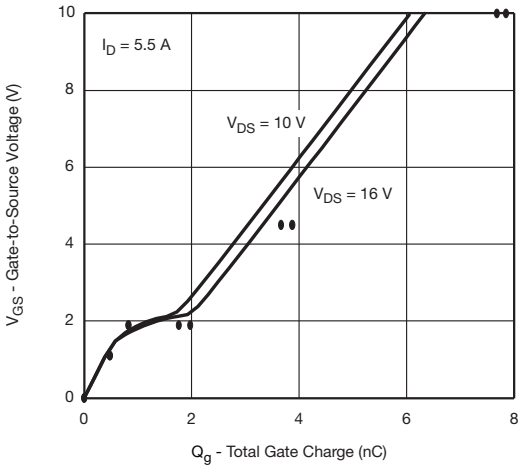
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted
N-Channel MOSFET

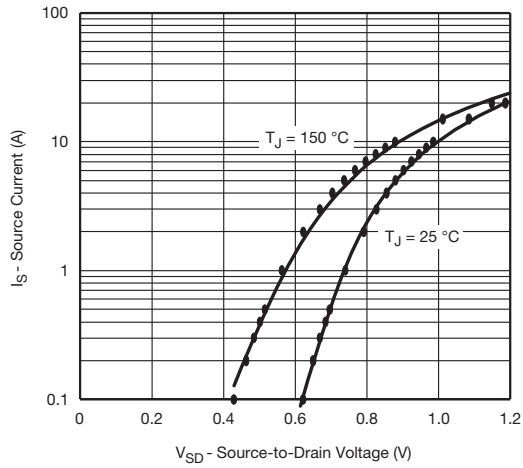








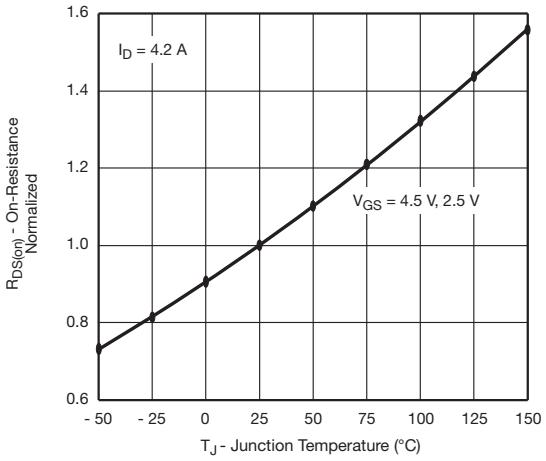


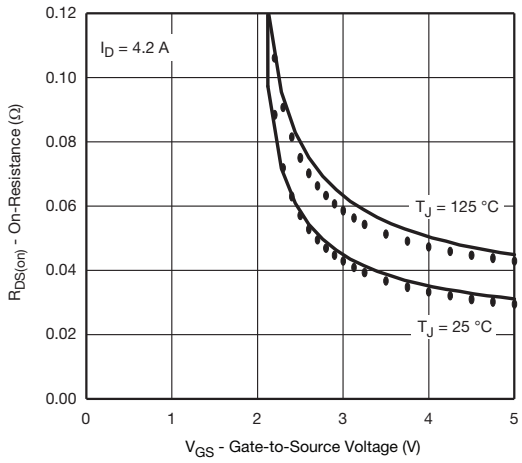


Note
Dots and squares represent measured data.

COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

N-Channel MOSFET





Note

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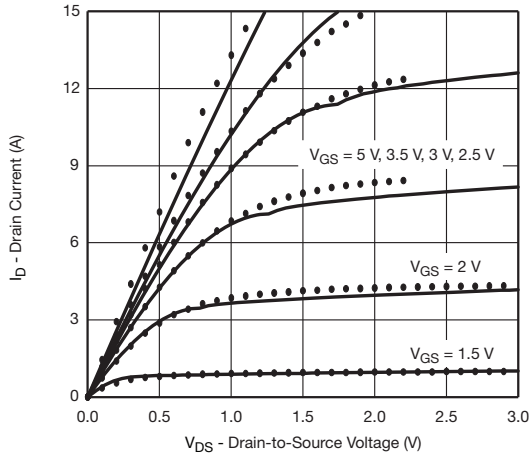
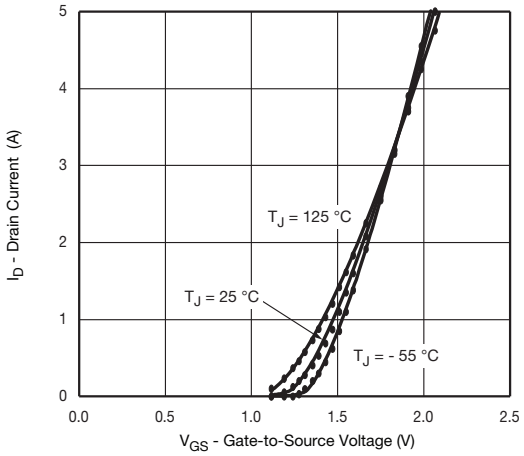
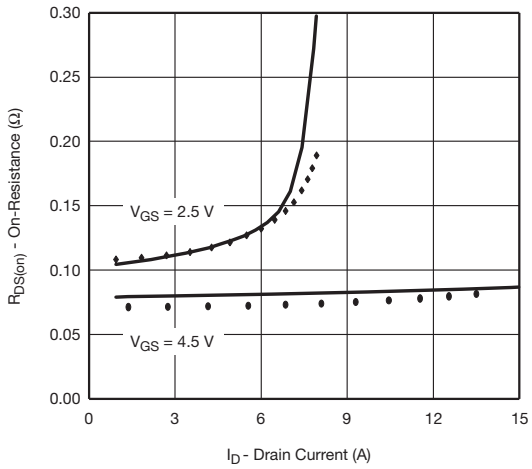
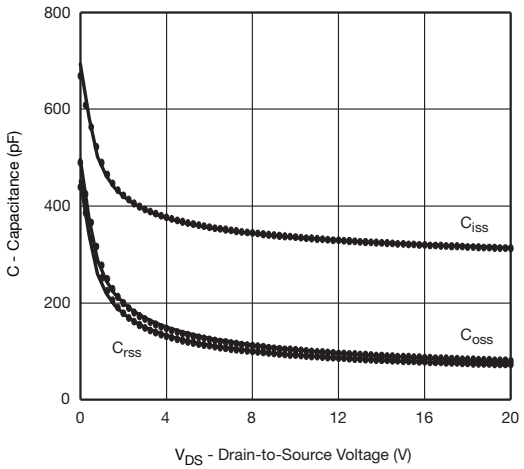
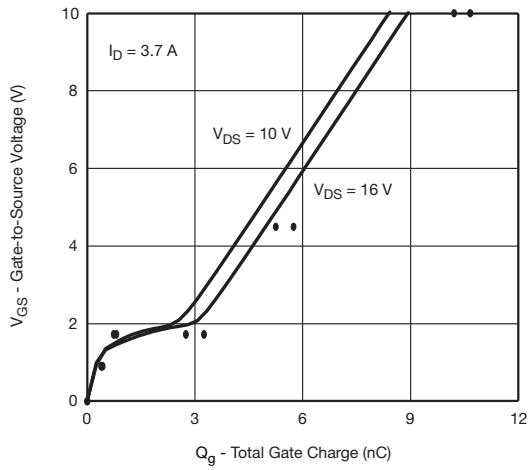
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted
P-Channel MOSFET

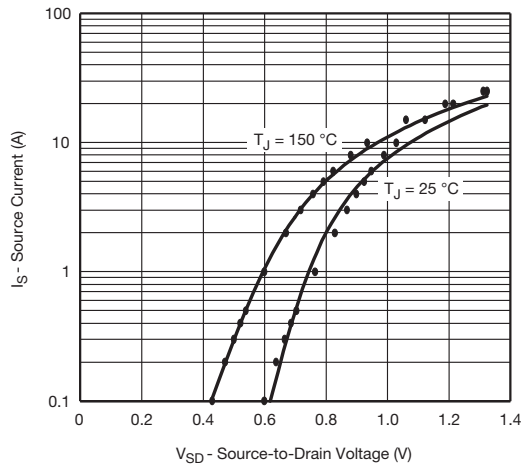












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